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APPLICATION FOR U.S. LETTERS PATENT

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Title:

**METHOD FOR MEASURING REGISTRATION
OF OVERLAPPING MATERIAL LAYERS
OF AN INTEGRATED CIRCUIT**

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METHOD FOR MEASURING REGISTRATION

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Field of the Invention

The present invention relates to semiconductor processing, and in particular, to a method for measuring the registration between two or more integrated circuit layers.

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Background of the Invention

Semiconductor-based integrated circuits are typically manufactured through the formation of a set of layers on a wafer containing many integrated circuit areas that are later separated into individual dies. Very thin layers of material are deposited one on top of the other in patterns and

15 processed to form integrated circuit components.

One technique of deposition and patterning is photolithography where a material layer is first coated with a light-sensitive photoresist. The photoresist is exposed through a pattern mask of a desired circuit pattern. Depending upon the type of photoresist used, the exposed photoresist is

20 developed to remove either the exposed or unexposed resist. Etching and/or deposition processes are then used to create the desired circuit within the pattern created.

In most cases, the pattern mask should be precisely aligned on a wafer during processing. The overlay of the mask, the measure of how

25 accurately the pattern mask is aligned, will often determine whether the wafer will be functional or must be discarded. Because each wafer may undergo numerous photolithography processing steps, the alignment of each pattern mask, especially the last ones used, is dependant upon the correct

alignment of earlier masks. Poor overlay may destroy the intended electrical properties of a circuit device on a wafer.

A common practice in registration, or matching in position, of overlying layers in a semiconductor wafer is to use metrology structures such as registration patterns or marks in each layer of the wafer in regions outside of a circuit region. In particular, the box-in-box registration pattern is commonly used today. This technique employs squares of different sizes on the layers to be registered. When the two layers are exactly matched in position, or registered, the squares are concentric. Any registration error produces a displacement of the squares relative to each other. To ensure ideal registration between masks, four box-in-box alignments are typically performed simultaneously, with the boxes located at the four corners of the image field.

Since semiconductor devices are expensive to fabricate, it is desirable to verify registration after the application of each layer. If the displacement of the layers is outside tolerable limits, sometimes the defective layer can be removed or replaced with an accurately registered layer. In other cases, the substrate is discarded so that further processing steps are not performed on a defective substrate. In any event, significant registration errors must be noted and corrected, otherwise subsequently fabricated wafers would likely have the same registration errors.

In the prior art, monitoring and verification of registration was done manually. Laboratory operators using microscopes examined the registration of overlying layers on each semiconductor wafer. Unavoidably, this technique was slow, subject to human errors and capable of producing substrate contamination.

Recently, the registration of overlying layers has been measured by automated systems, such as optical microscopy and scanning electron microscopy (SEM). For example, registration errors can be measured by a process in which an image of a set of registration patterns, such as box-in-box, recorded by a video camera through a microscope, are processed to obtain a measurement of the registration error.

As feature sizes and the alignment requirements of semiconductor devices shrink, the lens distortion of the exposure system has a larger impact on the alignment budget. Alignment errors due to lens distortions have been shown to be dependent on feature size and pitch. This size and pitch dependency can induce a measured alignment offset difference between the standard box-in-box method and the actual circuit layers of interest.

Accordingly, a method for measuring displacement between layers of a semiconductor wafer, which is inexpensive to implement, fast in operation and simple to automate is needed. There is also a need for a method that allows accurate measurement of layer registration errors, while avoiding the systematic errors associated with the prior art measurement systems.

Summary of the Invention

The present invention provides a method and apparatus that overcome some of the problems associated with registration measurements.

The present invention utilizes optical or scanning electron microscopy images of two or more overlying integrated circuit layers. The portion of the integrated circuit layers that is imaged contains the actual

operative circuitry of the chip. The respective images are digitized and the digitized patterns are further analyzed for the relative placement of the two layers. The measured offset of predetermined features in the layers can then be compared to a database containing previously computed data for what the

5   feature offset should be in the two layers. The difference between the imaged and the ideal placement, if outside a tolerable limit, is then used to correct processing errors or inefficiencies in the subsequent fabrication of other wafers.

The above and other advantages and features of the present

10   invention will be better understood from the following detailed description of the preferred embodiment which is provided in connection with the accompanying drawings.

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Brief Description of the Drawings

Figure 1 illustrates a registration measurement system according to one embodiment of the present invention.

20   Figure 2 is a block diagram of the illustration of Fig. 1.

Figure 3 is a flow diagram of the registration steps in accordance with the present invention.

25   Figure 4 represents features of such overlying material layers in a semiconductor device which is useful in explaining the invention.

Figure 5 illustrates an aerial image 2D contour of the overlying material layers of Figure 4.

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Detailed Description of the Preferred Embodiments

In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in 10 the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural, electrical and methodology changes may be made without departing from the invention. Accordingly, the following detailed description is not to be taken in a limiting sense and the scope of the present invention is defined by the 15 appended claims.

The present invention provides a method for measuring registration between overlying layers of a semiconductor wafer. The registration method measures the displacement of the actual patterns on the scanned semiconductor layers, rather than that of metrology structures such 20 as, for example, the set box-in-box pattern.

The present invention is implemented in a semiconductor device imaging system 100, an exemplary one being shown in Figures 1 and 2. The system 100 includes a prealigner 142 for handling cassette wafer holder 140, an automated imaging system 146, an image processor 148, and a computer 25 150 which further comprises one or more processors and associated memory,

an image monitor 152, a text screen 154, a keyboard 156, and a disk drive 158.

As illustrated in Figures 1 and 2, cassette wafer holder 140 contains semiconductor wafers to be measured and is mounted on system

5   100. A wafer transport system or a wafer handler (not shown) removes a semiconductor silicon wafer 10 from cassette 140 and places it on prealigner 142. A typical wafer transport system is a model CKG1 or CKG3 available from FSI. Semiconductor wafer 10 has a given size, typically ranging from 75 mm (3 inches) to 200 mm (8 inches) in diameter.

10   The wafer transport system further transfers semiconductor silicon wafer 10 from the prealigner 142 onto stage 118. Stage 118 can move in three dimensions and permits the positioning of semiconductor wafer 10 relative to the automated imaging system 146. Stage 118 may be any conventional device, such as a piezoelectrically driven stage, that provides

15   precise movement over a broad range of distances.

The automated imaging system 146 may be either an optical system or a scanning electron microscope (SEM), both being used in the present invention for generating aerial images of wafer 10.

The optical system could include a microscope and a video camera

20   positioned above semiconductor wafer 10. The microscope could carry objectives ranging in power from 2.5X to 200X magnification. For example, the microscope of the optical system could be a Zeiss Axiotron type and the video camera a Dage MT168 series.

Similarly, the present invention could use a scanning electron

25   microscope (SEM) as the imaging system 146. As described in the

background section of this application, a conventional SEM focuses an emitted electron beam toward the semiconductor wafer 10.

Referring now to Figure 3, a process for measuring material layer registration in a semiconductor device using the equipment shown in Figures 1 and 2 will now be described. After a system initialization at step 200, step 202 begins with the automated imaging system 146 taking a top-down image of a semiconductor wafer 10 at a predetermined step in the fabrication process and at a predetermined area of the circuit which may be user selectable. This image includes features of two or more layers of the wafer combined in a single top-down image. For purposes of simplification, we will assume that two material layers, a first and a second, are imaged. The first individual layer will have at least one predetermined featured reference point in the image.

For example, if the printed feature is a circular feature, the reference point might be the radial center of the radius of curvature of the feature or it could be a predetermined location along the edge of the feature. The reference point could also be a centroid of a feature or have some other spatial relationship to one or more features of the layer. Likewise, the second individual layer, which overlies the first will also have a predetermined feature reference point in the image. Figure 4 is a simplified drawing illustrating respective features 301 and 303 in two overlaid material layers in the aerial image. A predetermined feature reference point for feature 301 can be the center point 305, while a predetermined feature reference point for feature 303 can be a radial center point 307.

Although Figure 4 shows positions of two features, each having an associated reference point, it should be appreciated that additional features

and associated reference points can be used in each material layer, as exemplified in the aerial image taken in Figure 5. Also, although Figure 3 shows one reference point for each feature, it should be apparent that multiple reference points can be used for each feature of each layer.

5   The degree of alignment of the two layers is represented by the degree of alignment of the feature reference points. Taking the example shown in Figure 4, if the two featured reference points 305 and 307 are supposed to overlap when the material layer containing feature 301 is properly aligned with the material layer containing feature 303, the degree of

10   non-overlap of the reference points in the X and Y directions of a rectangular coordinate system represents the degree of misalignment of the two layers. That is, the values Δx and Δy in Figure 4 represent the degree of misalignment of the two layers.

Following the capture of a top-down image of at least two

15   overlying material layers in step 202, the process proceeds to step 204 where the feature reference points in the two material layers are located. The reference points can be located by an analysis of the images captured themselves that is, taking Figure 3 as an example, computer 150 takes the image from image processor 148 and finds the center points 305 and 307 of

20   the respective features 301 and 303 of the two overlapping material layers. Once the reference points are located the process proceeds to step 206, where the relative locations of those reference points in an ideal wafer is used as a basis for comparison with the actual locations of the featured reference points found in step 204.

25   The ideal relationship of the compared feature points can be found in the original design specifications for the circuit portion under

examination, or can be found from a previously imaged circuit where the reference points were in perfect alignment. In either case, at step 206 the computer determines whether the featured points, for example, 305 and 307 in Figure 3, are in the proper relationship, which would indicate proper

5   alignment of the two material layers. If the two featured reference points are not in the alignment they are supposed to be in, as determined from the database or ideal image, the degree of offset of the two is noted in a rectangular coordinate system and represented by a Δx and Δy value from where these two reference points are supposed to be located.

10   In Figure 4, for example, the reference points 305 and 307 are supposed to exactly overlap so that the degree of offset is easily represented by a Δx and Δy value. This Δx and Δy value represents then the degree of offset between the two material layers.

The process then proceeds to step 208 to determine whether any

15   offset that has been determined between the reference feature points is within a tolerable limit. If not, a registration error is indicated in step 206 and the magnitude of that error is noted. This can be in the form of a computer record which is generated, as well as an image presented on the image monitor 152 showing the degree of error on an actual depiction of

20   the image under investigation. Likewise, an offset of this magnitude can be displayed on text screen 154 and recorded on a recording medium by disc drive 158.

If the featured reference points are within tolerable limits of step 208, and in any event once step 210 is completed, the process returns to step

25   212 where the process determines whether there are other areas of interest on the captured image that need examination. If so, the process proceeds

from step 212 back to step 202, and another area of the image under consideration is then inspected and the process steps repeated. If at step 212 there are no other areas of interest for examination, the process proceeds to an end step 214.

Thus, the invention allows for a determination of a degree of misalignment of overlapped layers of an integrated circuit by actual inspection of an image showing the overlapped areas with a determination of the degree of alignment or misalignment, which is based on reference points provided in each of the two layers. As a consequence, the degree of misregistration of overlying layers can be directly determined rather than inferentially determined in a quick and efficient manner, and can be used whenever overlapping registration is a criticality in material layers of an integrated circuit under fabrication.
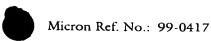
It should be readily apparent that the present invention can be used for any overlapping material layers at any area or site in a field of an IC as long as the examined area contains features from both layers which are in the obtained images, the locations of which can be identified by associated feature reference points.

While the invention has been described in detail with reference to semiconductor wafers, it should be readily apparent that the present invention can be used with other substrates having overlapping material layers as well.

While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of

variations, alterations, substitutions or equivalent arrangements not

described here, but which are commensurate with the spirit and scope of the

invention. Accordingly, the invention is not to be seen as limited by the

foregoing description, but is only limited by the scope of the appended

5   claims.

What is claimed as new and desired to be protected by Letters

Patent of the United States is: